IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Rajski et al.
Application No. 09/620,021
Filed: July 20, 2000
Confirmation No. 3823
For: CONTINUOUS APPLICATION AND DECOMPRESSION OF TEST PATTERNS TO A CIRCUIT-UNDER-TEST
Examiner: Phung M. Chung
Art Unit: 2133
Attorney Reference No. 1011-54375-01

CERTIFICATE OF MAILING

I hereby certify that this paper and the documents referred to as being attached or enclosed herewith are being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: MAIL STOP RCE, COMMISSIONER FOR PATENTS, P.O. BOX 1450, ALEXANDRIA, VA 22313-1450 on the date shown below.

Attorney or Agent for Applicants _____

Date Mailed 8-28-08

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INFORMATION DISCLOSURE STATEMENT PURSUANT TO 37 C.F.R. § 1.97(b)(4)

Listed on the accompanying form PTO-1449 and enclosed herewith are several English-language and/or non-English-language documents. Applicants respectfully request that these documents be listed as references cited on the issued patent.

Japanese Patent Publication No. 63-286780 describes a fault detecting system and fault detecting device. Japanese Patent Publication No. 03-012573 describes a logic circuit testing device having a test data changing circuit. Japanese Patent Publication No. 05-249197 describes an incorporated self-test circuit. Japanese Patent Publication No. 07-174822 describes a semiconductor integrated circuit device. Japanese Patent Publication No. 07-198791 describes a shared test register for simplifying integrated circuit testing and a built-in self-test (BIST) circuit using the same. Japanese Patent Publication No. 08-015382 describes a circuit incorporating a

self test function. Japanese Patent Publication No. 11-174126 describes a self-inspection pattern generation device for incorporation in a logic circuit and also describes a pattern selection method. Japanese Patent Publication No. 11-264860 describes an output circuit of a semiconductor device with test mode.

In the Examiner's April 23, 2008, Notice of Allowability, the Examiner suggests that the IDSs filed after the November 13, 2006, Supplemental Notice of Allowability failed to comply with 37 C.F.R. 1.97(d). At the time those IDSs were filed, however, Applicants understood that the November 13, 2006, Supplemental Notice of Allowability had been issued in error because no Notice of Allowance had been mailed by the Patent Office and because the Supplemental Notice of Allowability failed to address all pending claims in the application. Therefore, and as indicated by the Examiner during several telephone conversations, Applicants understood that the November 13, 2006, Supplemental Notice of Allowability was going to be withdrawn. To expedite prosecution, however, Applicants are filing a Request for Continued Examination together with this IDS, which includes the references previously cited but not initialed as having been considered by the Examiner. Applicants respectfully submit that they have complied with the requirements of 37 C.F.R. §§ 1.56, 1.97, and 1.98 and that the Examiner is required to consider the references. According to 37 C.F.R. § 1.97, for example, the IDSs "shall be considered by the Office." 37 C.F.R. § 1.97(b) and (c). MPEP 609 also explains that "[o]nce the minimum requirements of 37 CFR 1.97 and 37 CFR 1.98 are met, the examiner has an obligation to consider the information."

Copies of United States patents and United States published patent applications do not have to be provided to the Patent Office (37 C.F.R. 1.98(a)(2)(ii)). Copies of unpublished U.S. applications do not have to be provided, as long as the application is available on PAIR, as this

requirement of 37 C.F.R. § 1.98(a)(2)(iii) has been waived by the United States Patent and Trademark Office pursuant to the Official Gazette Notice on October 19, 2004 (1287 OG 163). Applicants will provide copies of such patents or applications upon request.

Applicants filed this Information Disclosure Statement ("IDS") before the mailing of a first Office action after the filing of a request for continued examination. As a result, no fee should be required to file this IDS. However, if the Patent Office determines that a fee is required for Applicants to file this IDS, please charge any such fees, or credit overpayment, to Deposit Account No. 02-4550.

The filing of this IDS shall not be construed to be an admission that the information cited in the statement is, or is considered to be, prior art or otherwise material to patentability as defined in 37 C.F.R. §1.56.

Respectfully submitted,

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